MINDFUL LEARNING

Essential Skills: VLSI and Embedded

Introduction:

In this course, we will explore and learn some of the essential skill set that is required for the VLSI and Embedded professionals.

Objectives:

By the end of this course, you should be able to:

1. Design digital hardware modules
2. Effectively use Verilog HDL constructs to model digital hardware modules
3. Have deeper understanding of the FPGA architecture
4. Explain and take any RTL design the FPGA design flow
5. Implement the RTL design on a given FPGA kit
6. Explain the verification flow
7. Analyze the design specifications and build a verification plan
8. Write test benches using Verilog HDL and Systemverilog HVL
9. Write appropriate test cases for the design under test
10. Understand coverage and achieve coverage goals for a given verification activity
11. Understand the importance of assertions and use them efficiently in test benches
12. Employ FPGAs for verification of RTL designs
13. Build Embedded Systems using FPGA using Picoblaze and Microblaze soft-processors
14. Implement RTOS based systems on FPGA
15. Implement processor IP and further explore SoC based designs on FPGA
16. Design MATLAB and Simulink Models
17. Write and analyze scripts in perl

Pre-requisites:

1. Digital logic
2. Knowledge of VHDL and /or Verilog HDL is desirable

Who should attend?

This course is meant for graduate, post-graduate students and fresh engineers who wish to develop their skill set in verification methodologies. It is beneficial for corporate people who wish to enhance their skill set for better opportunities.

Contents:

Stage 1:

1. Verilog HDL Review
    1. Fundamentals of Verilog HDL
    2. Constructs in Verilog for hardware modeling
    2. Modeling Combinational and Sequential Digital Systems
    3. Modeling Finite State Machines (FSMs)
    4. Modeling memories such as RAMs, ROMs and FIFOs in Verilog
2. Verification fundamentals and verification flow
3. Writing automatic test benches in Verilog

Stage 2:

Systemverilog for RTL Verification

1. Language constructs
2. Arrays and queues
3. Tasks and functions
4. Mailboxes and semaphores
5. Interfaces and clocking blocks
6. OOP constructs
7. Randomization
8. Coverage constructs
9. Fundamentals of assertions
10. Mini-project (Wishbone IP)

Stage 3:

FPGA flow

1. FPGA architecture
2. Xilinx Design Tools
3. Design Entry and Simulation
4. Synthesis
5. Pin Configuration
6. Timing Constraints and Analysis
7. Porting and testing the design on FPGA
8. Debugging with Chipscope

Stage 4:

SoC design principles on FPGA

1. Introduction to processor design in FPGA
    a. Case study: Design of the Gumnut processor
2. Introduction to system busses
3. Introduction to protocols
4. Introduction to peripheral IP design

Stage 5:

Embedded Systems on FPGA

1. Introduction to Picoblaze processors
2. Embedded systems design on FPGA using Microblaze softprocessors
3. RTOS on Microblaze

Stage 6:

Working with MATLAB and Simulink

1. MATLAB features
2. Language constructs
3. Plotting and other graphical features
4. Control flow
5. Scripts and functions
6. Working with Simulink

Stage 7:

Scripting with perl

1. Introduction to *perl*
2. Operators, literals and variables
3. Arrays and Hashes
4. Sub-routines
5. References
6. Statements and loops
7. Debugging
8. Regular expressions
9. Special variables
10. File I/O and directory operations
11. Reports
12. Perl Modules
13. Introduction to networking in *perl*
14. Working with databases

Cost:

Rs. 35000/-

Please contact us for discounts for multiple participants.

Mode of delivery:

1. Class-room sessions
2. Online